REMARKS

Applicants thank the Examiner for the careful consideration given to this application.

Claims 20, 24, 35, 37, 50-51 and 54-55 are pending in this application. Claim 37 is the sole independent claim. Claim 53 is canceled without prejudice or disclaimer. Claims 1-19, 21-23, 25-34, 36, 38-49 and 52 were previously canceled without prejudice or disclaimer.

Claim Rejections under 35 U.S.C. §102

Claim 53 stands rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,066,581 to Chivukula (hereinafter "Chivukula").

Without conceding the merits of this rejection, claim 53 has been canceled, solely for the purpose of advancing prosecution, thereby rendering the rejection of claim 53 moot.

Therefore, Applicants respectfully request that this rejection of claim 53 under 35 U.S.C. §102 be withdrawn.

Claim Rejections Under 35 U.S.C. §103

Claims 20, 24, 35, 37, 50, 51, 53, 54 and 55 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2002/0137260 to Leung (hereinafter "Leung") in view of U.S. Patent No. 5,900,223 to Matijevic (hereinafter "Matijevic").

Claim 54 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Leung in view of Matijevic, and in further view of U.S. Patent No. 5,143,637 to Yokouchi (hereinafter "Yokouchi").

As mentioned above, without conceding the merits of the rejection, claim 53 has been canceled thereby rendering this rejection of claim 53 moot.

With regard to the remaining claims, Applicants submit that the rejections have been overcome by the attached executed Declaration Under 37 CFR 1.131 and Exhibit.

The Declaration along with the Exhibit verify that the present inventors reduced to practice the invention disclosed and claimed in the United States prior to January 11, 2001, which is the filing date of Leung, the primary reference relied upon in the above rejection. In particular, the Declaration states that prior to January 11, 2001, the invention disclosed and

claimed in the present application was conceived by the inventors in the United States and was reduced to practice by them and/or under their direction and/or supervision. Especially, a dielectric thin film with relative dielectric constant greater than 10 consisting essentially of a solution or dispersion of surfactant-coated nanoparticles in an organic solvent, wherein the organic solvent is evaporated after heating and depositing the nanoparticles on a substrate to form the dielectric thin film, wherein nanoparticles have a diameter size in a range between 2 nm and about 20 nm, and a crystalline structure having a relatively narrow grain-sized distribution, wherein the narrow grain-sized distribution has a standard deviation selected from the group consisting of less than 15%, less than 10% and less than 5%.

The filing of the Declaration Under 37 CFR 1.131 is not to be construed as an admission, estoppel or acquiescence to the rejections. Please see *Credle v. Bond* 23 F. 3d 1566; 30 USPQ 2d. 1911 (Fed. Cir. 1994) and *Greenwood v. Hattori Seiko Co. Ltd.* 14 USPQ2d 1474, (Fed. Cir. 1990).

Furthermore, none of the remaining references, Matijevic and Yokouchi, taken alone or in combination, disclose or render obvious the present invention.

In view of the above, Applicants respectfully request that this rejection of claims 20, 24, 35, 37, 50, 51, 53, 54 and 55 under 35 U.S.C. §103 be withdrawn.

Disclaimer

Applicants may not have presented all possible arguments or have refuted the characterizations of either the claims or the prior art as found in the Office Action. However, the lack of such arguments or refutations is not intended to act as a waiver of such arguments or as concurrence with such characterizations.

CONCLUSION

In view of the above, consideration and allowance are respectfully solicited.

In the event the Examiner believes an interview might serve in any way to advance the prosecution of this application, the undersigned is available at the telephone number noted below.

The Office is authorized to charge any necessary fees to Deposit Account No. 50-0510.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0510, under Order No. YOR920010225-US2 from which the undersigned is authorized to draw.

Dated: September 22, 2010

Respectfully submitted,

Electronic signature: /Burton A. Amernick/
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Attorneys for Assignee

Docket No.: YOR920010225US2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Charles T. Black et al.

Application No.: 10/784,591 | Confirmation No.: 9561

Filed: February 23, 2004 | Art Unit: 2818

For: METHOD FOR FABRICATING CRYSTALLINE-DIELECTRIC THIN FILMS AND DEVICES FORMED USING SAME | Examiner: D. J. Goodwin

DECLARATION UNDER 37 C.F.R. §1.131

Charles Black and Christopher Bruce Murray declare that they are joint inventors of the subject matter which is disclosed and claimed in U.S. patent application Serial Number 10/784,591, which was filed in the United States Patent and Trademark Office on February 23, 2004, which claims the benefit under 35 USC 120 to parent application Serial Number 10/266,000, filed in the United States Patent and Trademark Office on October 7, 2002, now US Patent 6,737,364, and that they reduced to practice inventions disclosed and claimed in the United States prior to January 11, 2001, the filing date of US Patent Application 09/761,529 to Leung et al.; and further state as follows:

Prior to January 11, 2001, the inventions disclosed and claimed in the above identified U.S. Patent Application were conceived by us in the United States and were reduced to practice by us and/or under our direction and/or supervision. Especially, a dielectric thin film with relative dielectric constant greater than 10 consisting essentially of a solution or dispersion of surfactant-coated nanoparticles in an organic solvent, wherein the organic solvent is evaporated after heating and depositing the nanoparticles on a substrate to form the dielectric thin film, wherein nanoparticles have a diameter size in a range between 2 nm and about 20 nm, and a crystalline structure having a relatively narrow grain-sized distribution, wherein the narrow grain-sized distribution has a standard deviation selected from the group consisting of less than 15%, less than 10% and less than 5%.

This is further evidence by Exhibit A (copy attached), which is a true copy with the dates being redacted of the relevant portions of IBM Invention Disclosures for YOR20010225US2. All of the dates that have been redacted are prior to January 11, 2001.

It is not possible to produce the signatures of the inventors Charles Black and Christopher Bruce Murray. Both Charles Black and Christopher Bruce Murray were employees of International Business Machines Corporation and assigned their rights to International Business Machines Corporation. Pursuant to MPEP 715.04(I)(D), the Declaration has been executed by the assignee, International Business Machines Corporation, on behalf of the unavailable inventors.

We hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned is authorized to act on behalf of the assignee, International Business Machines Corporation:

September 22, 2010
DATE

Pryor A. Garnett, Reg. No. 32,136
Senior Counsel, International Business Machines Corporation

Disclosure YOR8-1998-0721
Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Charles Black On [redacted]
Last Modified By wpts1 wpts1 On 03/28/2010 04:15:48 PM CDT
Archived on 06/08/2002

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

*** Title of disclosure (in English)**
Method for Fabricating Crystalline-Dielectric Thin Films

Summary

Status	Final Decision (File)
Final deadline	
Final deadline reason	
Docket family	YOR9-2001-0225
* Processing location	Yorktown
* Functional area	700 Systems, Technology & Science-Isaac
Attorney/Patent professional	Casey August/Watson/IBM
Business Area Manager/IDT Lead	
Evaluators	
Submitted date	11/13/1998 03:53:53 PM EST
* Owning division	RES
Incentive program	

9/2/2010

Lab
* Technology code
Patent value tool (PVT) score

To calculate a PVT score, answer all of the questions in the "Patent Value Tool" section below, then click on the Calculate "PVT" action button.

Inventors with a Blue Pages entry

Inventors: Charles Black/Watson/IBM, Christopher B Murray/Watson/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Black, Charles (Chuck) Murray, Christopher B.	846154 707272	22/K3QB 22/LEJA	N/A N/A	Tiwari, Sandip Scott, Bruce A.

> denotes primary contact

Inventors without a Blue Pages entry

Invention Development Team Information

Attorney/Patent professional	Casey August/Watson/IBM
Business area manager/IDT lead	
Evaluators	
Other interested parties who may view this disclosure	
Date evaluation response due to IP Law	

Main Idea

To view the Main Idea of this disclosure, open the "Main Idea" document from the view

***Critical Questions (Questions 1-9 must be answered in English)**

*	**Question 1** On what date was the invention workable? [redacted] **Please format the date as MM/DD/YYYY** (Workable means i.e. when you know that your design will solve the problem)	
*	**Question 2** Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	
	If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
	Are you aware of any publications, products or patents that relate to this invention?	
	If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
*	**Question 3** Has the subject matter of the invention or a product incorporating the invention	

	been sold, used internally in manufacturing, announced for sale, or included in a proposal?	
	Is a sale, use in manufacturing, product announcement, or proposal planned?	
	If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made. Product: Version/Release: Code Name: Date: To Whom: If more than one, use cut and paste and append as necessary in the field provided.	
*	**Question 4** Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers?	
	If yes, give a date. **Please format the date as MM/DD/YYYY**	
*	**Question 5** Have you ever discussed your invention with others not employed at IBM?	
	If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.	
*	**Question 6** Was the invention, in any way, started or developed under a government contract or project?	
	If Yes, enter the contract number	
*	**Question 7** Was the invention made in the course of any alliance, joint development or other contract activities? If **Yes**, enter the following:	
	Name of Alliance, Contractor or Joint Developer	
	Contract ID number	
	Relationship contact name	
	Relationship contact E-mail	
	Relationship contact phone	
*	**Question 8** Have you, or any of the other inventors, submitted this same invention disclosure or similar invention disclosure previously?	
	If Yes, please provide disclosure number below: submitted to Casey August in paper form several months ago. Maybe [redacted]	
*	**Question 9** Are you, or any of the other inventors, aware of any related inventions disclosures submitted by anyone in IBM previously?	
	If Yes, please provide the docket or disclosure number or any other identifying information below:	
	Question 10 What type of companies do you expect to compete with inventions of this type? *Check all that apply.* Manufacturers of computer memory hardware	

(Form Disclosure, Revised 01-Dec-2006)

Main Idea for Disclosure YOR8-1998-0721
Prepared for and/or by an IBM Attorney - IBM Confidential

Archived On 03/13/2001 02:01:00 AM

Title of disclosure (in English)
Method for Fabricating Crystalline-Dielectric Thin Films

Main Idea

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.
This invention describes a new method for forming and depositing thin films of crystalline dielectric materials. Our technique uses chemical synthesis to control the granularity and thickness of the dielectric films. This method has several key advantages over existing technologies, and it will facilitate the integration of crystalline dielectric materials into high-density memory devices.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
In recent years there has been significant effort focused on integrating perovskite-type insulators (most notably Barium Strontium Titanate, or BST) into high-density DRAM memory structures. These materials are crystalline dielectrics, which exhibit large dielectric responses (relative to conventional amorphous dielectrics such as SiO2) due to ionic displacements within their crystal lattice. Similarly, there have been renewed efforts to develop viable high-density, non-volatile memory circuits based on ferroelectric dielectrics. Ferroelectric materials are also crystalline dielectrics, and they possess the additional property of a permanent electric dipole moment. From a fabrication standpoint, combining these dielectrics with silicon processing poses serious difficulties. Forming the proper crystal structure (to obtain desired dielectric properties) requires high processing temperatures which can have a determintal effect on other parts of the circuit. Also, because these dielectrics are crystalline, the film's grain structure and orientation play a crucial role in determining device characteristics such as leakage and polarization. In this Disclosure we propose a new and very general method for processing crystalline dielectrics which naturally avoids several of the issues hindering their integration into standard silicon processes. We believe our process will be most helpful in facilitating the integration of ferroelectric thin films, but it may also prove useful in processing other crystalline dielectrics such as BST.
One main obstacle in the development of thin perovskite insulating films is in controlling the film's grain structure. Upon crystallization to the perovskite phase (which is the phase needed to obtain a high dielectric constant), the film forms grains which are typically on the order of 0.1-1 μm in diameter. Recent work has shown that the grain size in these films (in particular, much work has been done on BST) can be influenced somwhat by film deposition conditions. Additionally, upon crystallization to the high-dielectric phase, some films can become quite porous. Voids between grains in the dielectric can cause electrical shorts for sufficiently thin films. Problems associated with film grain size have become important as we attempt to build

devices which are roughly the same size as the film granularity.
The main integration problem for crystalline dielectrics is illustrated in Figure 1. Dielectrics of this type which are deposited by conventional means typically require annealing at high temperatures (> 600 C) in the presence of oxygen in order to form the proper crystalline phase (i.e. - high dielectric phase). The consquences of this annealing step, which are shown in the Figure, can have a detrimental effect on the memory device.
In a high-density memory device, the capacitor is connected to a transistor (the two compose the memory device) via a conducting plug, which is typically made of polycrystalline silicon (poly-Si) (see side-view in Fig. 1). The vertical plug allows the capacitor to be positioned directly above the transistor, thereby saving areal density on the wafer. (In lower-density memory structures the capacitor and transistor can exist side-by-side on the wafer surface, which alleviates the difficulty described here.) When this structure is heated to >600 C in an oxygen atmosphere, oxygen diffuses through the bottom electrode and down to the conducting plug. Once in contact with the plug, oxygen reacts with the Si, forming an insulating SiO2 layer and effectively disconnecting the transistor from the capacitor. A large effort is currently focussed on developing a conducting barrier layer to place between the bottom capacitor electrode and the poly-Si plug. The requirements for such a barrier are stringent: it must be electrically conducting, stop oxygen diffusion, and be non-reactive with oxygen at temperatures up to >600 C.
These problems are major obstacles to the development high-density memory devices using crystalline dielectrics. We now describe a technique for using chemical synthesis to form a crystalline dielectric in solution, completely separate from the rest of the circuit. Only after the dielectric is synthesized and crystallized in the proper form (as a uniform ensemble of nanometer-scale clusters) is it selectively deposited into the desired area of the silicon circuit.

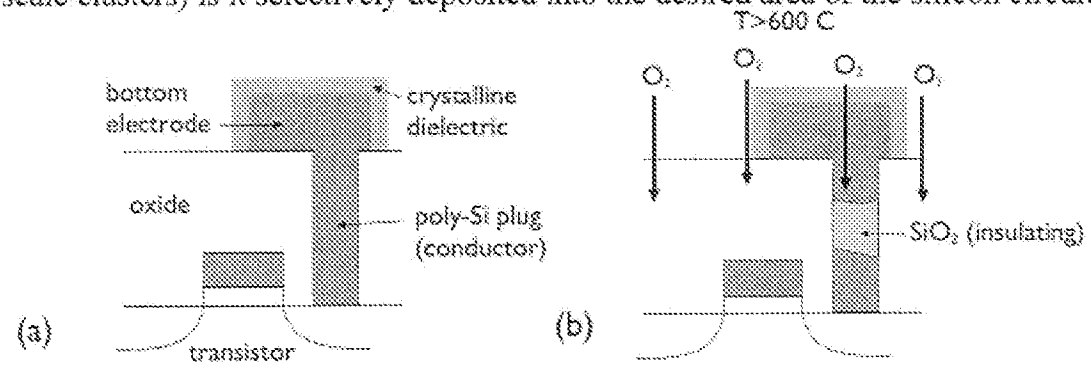

FIGURE 1: (a) side-view schematic of a high-density memory device. (b) In order to form the proper dielectric crystal phase, the device is subjected to a high-temperature oxygen anneal. Diffusion of the oxygen down to the poly-Si plug can lead to the formation of an insulating layer, making the device inoperable.

OUR TECHNIQUE
In order to circumvent the problems outlined above, we propose an entirely new method for making thin films of crystalline dielectrics. Rather than relying on more conventional techniques of thin-film deposition (evaporation, sputtering, chemical-vapor deposition, solultion-gelation deposition), we use chemical synthesis and self-assembly to controllably produce well-ordered thin films.
An outline of our technique is described as follows: Appropriate chemical precursors are reacted in solution to form small aggregates of the desired composition and crystal structure. By adjusting the chemistry in solution, we control the maximum size of the nanoparticles, and can also prevent them from agglomerating by coating with an organic layer. Once the reaction is complete, the particles can be size-selected using centrifuge techniques. This results in a solution containing

isolated, highly-uniform particles of the appropriate composition.
We make extremely thin films of this material by depositing the solution onto a solid substrate, and then evaporating the solvent (this step is shown in Fig. 2(a)). By choice of organic coating material, we control the spacing between the particles, and can also selectively deposit material onto different areas of the substrate. Most importantly, the particles self-assemble into close-packed arrays on the surface. After this step, further film processing may involve thermal treatments to remove the organic layer from the films (Fig. 2(b)), and also a sintering step to form a continuous film from the particles (Fig. 2(c)). Because the film is composed of nanoparticles and thus has a large surface area, we expect the sintering temperature for the film to be reduced far below its bulk value. Notice that the film thickness and grain size are precisely controlled by the diameter of the particles formed in solution. Thicker films can be made by repeating this procedure multiple times.
It is worth emphasizing here the numerous advantages of this technique, and the improvements it offers over more conventional approaches to making thin films of crystalline dielectrics. Most importantly, the formation of the correct crystal phase is done in solution, completely separate from the rest of the Si circuit. High-temperature annealing therefore does not impact the performance of the circuit, as the dielectric film is deposited into the circuit at low temperature and in the proper phase. This technique offers precise control of the film grain size (down to ~1 nm), which should help the formation of thin insulating dielectrics, and will be a big aid to their integration into nanometer-scale device structures. Additionally, for the case of ferroelectric films, we can control the orientation of the grains, and can thus align the ferroelectric polarization in the most desirable direction.

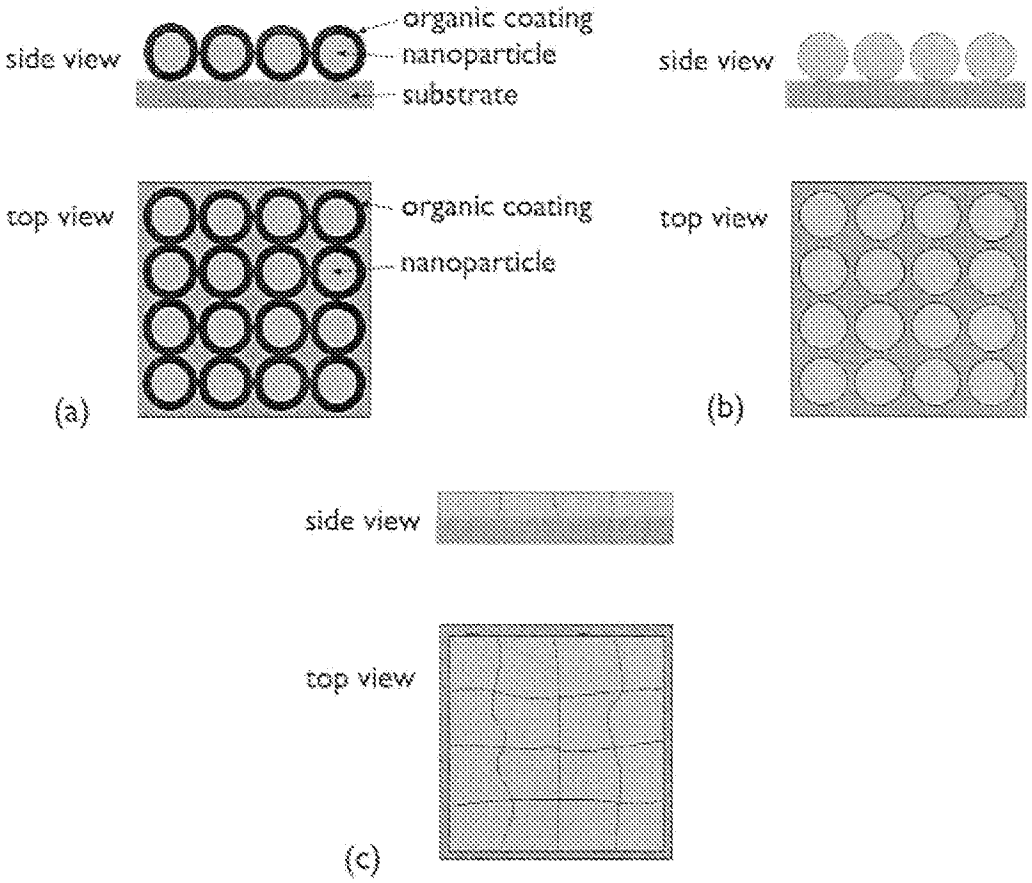

FIGURE 2: Thin-film formation (a) Arrays of organic-coated nanoparticles are deposited onto a surface. (b) A subsequent heat treatment removes the organic coat, leaving a well-ordered array of crystalline particles. (c) A final sintering step leaves a thin film of the dielectric. The grain size and the film thickness are controlled by the size of the particles initially deposited onto the surface.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Charles T. Black and Christopher B. Murray

Application No./Patent No.: 10/784,591 Filed/Issue Date: February 23, 2004

Titled: METHOD FOR FABRICATING CRYSTALLINE-DIELECTRIC THIN FILMS AND DEVICES FORMED USING SAME

International Business Machines Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made) the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 013367, Frame 0482, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[ ] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature _____ Sept. 22, 2010
Date

Pryor A. Garnett, USPTO Reg. No. 32,136 Senior Counsel
Printed or Typed Name Title